FULL-WAFER ROLLER-NIL PROCESSES FOR SILICON SOLAR CELL TEXTURISATION

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ABSTRACT: The highest solar cell efficiencies both for c-Si and mc-Si were reached using template based texturing processes. Especially for mc-Si the benefit of a defined texture, the so called honeycomb texture, was demonstrated impressively. However, up until now, no industrially feasible process has been available to pattern the necessary etching masks with the sufficient resolution. Roller-Nanoimprint Lithography (Roller-NIL) has the potential to overcome these limitations and to allow high quality pattern transfers, even in the sub-micron regime, in continuous in-line processes. Therefore, this etch-mask patterning technique is a suitable solution to bring such elaborate features like the honeycomb texture to an industrial realization. Beyond that, this fast printing-like technology opens up new possibilities to introduce promising concepts like photonic structures into solar cells.
Keywords: Texturisation, Light Trapping, Nanoimprint Lithography

1 INTRODUCTION

Surface textures are applied in silicon solar cells to reduce optical losses. These can mainly be divided in reflection and transmission losses. In high-efficiency laboratory scale solar cells defined textures are applied to achieve the best possible optical behavior [1, 2]. However, photolithographic processes used in laboratory are not applicable in industrial scale environments. Therefore, several research groups are searching for processes that on the one hand allow the fabrication of tailored surface patterns, but on the other hand maintain industrially feasible processing.

Investigated approaches can be divided into self-assembly and template based processes. Self-organized processes are e.g. the formation of hexagonal or opaline patterns achieved by coating processes of monodisperse spheres [3]. Template based or direct writing processes offer more degrees of freedom for the definition of patterns and can be found in a wide plurality of different processes in the literature. Most have in common, that the texturing process is conducted in two steps. Prominent examples for these so called top-down processes used for solar cell texturisation are: direct laser ablation [4] or laser ablation of etching masks [5] and inkjet patterning of etching masks [6, 7].

We investigate nanoimprint lithography (NIL) processes to pattern etching masks. NIL is based on the mechanical patterning of polymeric etching masks. This process is very similar to classical hot embossing, except that the polymeric layer has to be very thin to allow very low residual layer thicknesses after the imprint process. This patterned polymer layer can be used afterwards as an etching mask. The process was first introduced based on hot embossing of a thermoplastic polymer layer [8] and was then extended to UV-curing polymer materials to allow shorter cycle times [9]. To be able to conduct this process on large areas, it is essential to use soft stamp materials [10]. A step forward towards the industrial applicability of NIL processes is the development of a continuous Roller-NIL process. The development of this Roller-NIL tool at Fraunhofer ISE is described in [11]. Compared to the alternative processes mentioned before, a challenging aspect for NIL is that it is not a contact free process. However, in terms of throughput, resolution and definition of profile shapes, the other processes cannot compete with NIL.

Within this work we present two exemplary types of surface textures realized by the use of NIL processes. First, the front-surface honeycomb texturing of multicrystalline silicon will be described. There, a hexagonal pattern of around 10 microns period is realized, which can mainly be described by geometrical optics. This type of texture was applied when reaching the highest efficiencies on multicrystalline silicon up to now [2]. The second, a more demanding concept with regard to process development, is the realization of a diffractive structure on the rear side of silicon solar cells. This concept was first presented by Heine and Morf [12]. Already in their work, NIL-like processes were mentioned to potentially substitute elaborate processes like e-beam lithography, which were initially used to realize such patterns. This type of texture requires wave optical considerations for the design as well as the understanding of optical effects introduced by the gratings. The experimental works presented in this study are based on calculations for optimal grating parameters published in [13, 14].

2 PROCESS CHAIN

2.1 Master and stamp fabrication

Both applications, the honeycomb texturing as well as the diffractive rear side grating, are based on the use of periodic patterns. For the origination of periodic patterns on large areas, interference lithography (IL) is a very well suited technology. An overview of possibilities offered by IL can be found in [15], [16]. In IL a laser beam is split into two or more beams, which are expanded and superimposed on a photoresist coated sample. As result of the coherent and monochromatic radiation a very precise interference pattern can be transferred into the photoresist, so that after a development process a surface relief results. We use an argon-ion laser operated at 364 nm, which allows the origination of patterns with periods down to around 200 nm. The surface reliefs can be replicated into more stable and durable metal replications by electroplating processes (most often made of nickel). These so-called nickel shims can be used to establish non-wearing replication processes into soft-polymeric materials as e.g. PDMS in order to fabricate stamps for the NIL process. The PDMS replication is conducted using cast molding of thermally assisted addition curing silicone components. Besides the pattern

fidelity of the replication process, other important characteristics of the PDMS material are its UV-transparency for the latter UV-curing of resist as well as its elasticity. The elasticity can be quantified by the Young`s modulus; it has to be sufficiently high to ensure stability of the stamps features and hence no collapse of the pattern. On the other hand the material has to be soft, to guarantee a sufficient conformability to non-flat surfaces. This is essential to allow a large area imprinting process.

2.2 Nanoimprint lithography (NIL)

In the NIL process, as conducted within this study, a UV-curing of polymeric resist material is realized, while a PDMS stamp is pressed into this resist. We developed two tools for these NIL processes in house. The first is a conventional NIL tool based on a planar stamp setup, which is restricted to maximum substrate sizes of 100x100 mm². This tool is applied for process development and testing of resist materials. The second is a Roller-NIL tool, which is aimed at up-scaling NIL processes. Using this tool, rough silicon wafers of area 156x156 mm² can be imprinted homogeneously. Currently, we still apply spin coating for the resist coating. A next step towards industrial applicability will require an in-line resist coating process. Typical pressures during the imprint process for both tools are around 0.6 bar. That NIL is not contact free is often regarded as critical, especially for the handling of very thin silicon wafers. However, compared to screen printing processes, due to the use of soft stamp materials a very homogeneous pressure distribution can be achieved. The most critical process step is the demolding. This step was found to be far superior for the novel Roller-NIL tool compared to a conventional NIL setup. In the roller processing, the demolding takes place in a very continuous and defined peel-off of the stamp. Thereby, as little as 100 µm thick 125x125 mm² multicrystalline silicon substrates were imprinted without finding problems in terms of wafer breakage. Fig. 1 shows a photograph of the Roller-NIL tool developed at Fraunhofer ISE.

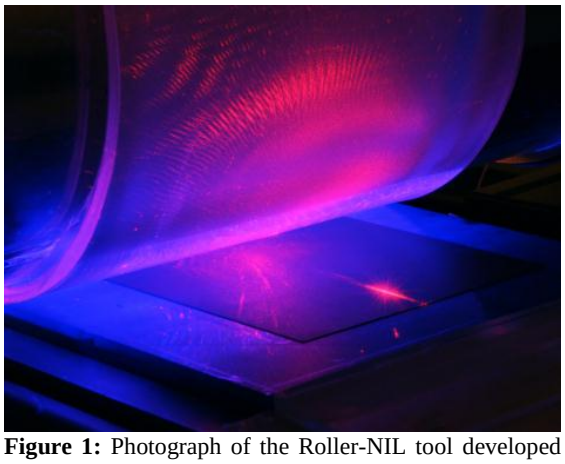

Figure 1: Photograph of the Roller-NIL tool developed at Fraunhofer ISE imprinting a 125x125 mm² multicrystalline silicon wafer.

2.3 Pattern transfer via etching

The imprinted resist layer typically features a thin residual layer beneath the etch mask pattern. Therefore, these imprinted etching masks are very well suited for the use of plasma etching processes. However, in principle wet chemical processes should also be possible. Up to now, adhesion of resist layers was found to be critical, so that a wet chemical etching for the pattern transfer into silicon was not successful.

Within this study, a plasma etching chamber was used, within which two different sources for plasma excitation are available. These are a radio frequency (RF) source, which can be used to couple in power capacitively via a parallel plate setup, and a microwave (MW) source, which allows an incoupling of power via a slot antenna. These sources allow different types of etching mechanisms. The parallel plate setup allows anisotropic reactive ion etching processes and the MW source allows a low damage isotropic etching of silicon. Etching processes investigated within this work are based on fluorine plasma chemistry as sulfur hexafluoride is used to provide reactive species. The sample plate used within the plasma tool allows a maximum substrate size of 125x125 mm².

3 HONEYCOMB TEXTURE

3.1 Master and stamp fabrication

For the honeycomb texture, master structures were originated using three-beam interference lithography. The masters were processed on 250x250 mm² glass substrates as described in [11]. For the stamp replication, a commercially available two component addition curing PDMS system was applied leading to a Young`s modulus of the stamp material of around 2 MPa. This soft material is perfectly suited for the replication of these relatively large patterns of around 8 µm period and pattern depth on very rough multicrystalline silicon substrates.

3.2 Nanoimprint lithography and plasma etching

The etching masks for this application were replicated using the Roller-NIL tool on large areas up to 156x156 mm². However, the further plasma etching processing is limited to sizes of 125x125 mm², as mentioned before. The resist is a free-radical curing solvent-free system, which is applied in a film thickness of around 3 µm. The hexagonal pattern of the etching mask has a depth of about 7 µm.

In the following, we describe the etching sequence, which comprises of reactive ion etching (RIE), plasma removal of the resist and isotropic MW plasma etching. Within the RIE process, oxygen (O_2) and sulfur hexafluoride (SF_6) are used as gases. The process conditions are set so as to avoid overly high acceleration voltages. Thereby, damages due to heavy ion bombardment can be limited. One way to do this, is to operate at high chamber pressures. This leads to small mean free path lengths of ions and electrons and thereby the bias voltage can be kept low. The challenge then is to achieve an effective side wall passivation during the RIE process to still be able to achieve anisotropic etching behavior. Fig. 2 shows an SEM micrograph of an etching pit with the remaining etching mask on top of it. It can be seen that even for pressures as high as 20 Pa very anisotropic etching behavior can be achieved.

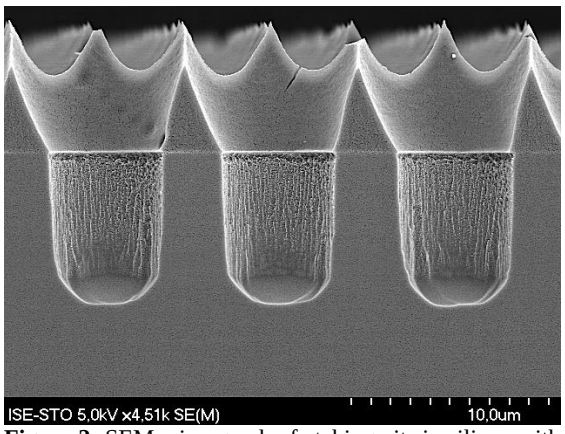

Figure 2: SEM micrograph of etching pits in silicon with the remaining resist mask after reactive ion etching.

After the RIE process, the resist mask is removed in a plasma ashing process. It was found that for cross-linking resist material only very low ashing rates can be achieved. Therefore, a design of experiments (DoE) was conducted on the basis of Ref. [17]. In this reference, it was already shown that adding a small amount of CF_4 to the O_2 ashing rates of cross-linked resist materials can be enhanced drastically. The DoE lead to very high removal rates of around 2.3 µm/minute, compared to around 100 nm/minute before the introduction of CF_4.

After the resist removal, etching pits are widened in an isotropic MW plasma process solely based on SF_6 as the etching gas. It is essential to apply the correct process time so that planar areas are minimized but the etching pits are not yet leveled.

3.3 Optical and electrical characterisation

Honeycomb textures of a very high optical quality were fabricated by the presented process chain. It was already reported that values for weighted reflectance of 12.5 % and 14.6 % were achieved on mono- and multicrystalline silicon respectively without ARC [11]. These values were achieved using the conventional NIL tool. In the same work, it was also shown on small cells that short circuit current densities on high efficiency FZ material were as high as 40.1 mA/cm² and 40.7 mA/cm² for a single and double layer ARC respectively. These values confirmed the high efficiency potential of the process chain on small areas.

Now, this process has been transferred to large area processing using the Roller-NIL tool (125x125 mm²). Even lower values for weighted reflectance (14.3 %) on multicrystalline silicon were achieved without ARC. As the next step, the influence of the texturisation process on the electrical quality was investigated. A special focus was set on the influence of the plasma ashing of the resist, because this process step was newly inserted into the process chain during the up-scaling. Sample preparation was done on 125x125 mm² 1 Ωcm p-type FZ material. The samples were texturized using the presented process chain and reference samples were left planar or textured with random pyramids. Also, a planar sample was processed that experienced solely the plasma ashing process to isolate potential influences. A $POCl_3$ diffusion was applied to introduce a 120 Ω/Sq emitter. The diffused samples were passivated by a 10 nm thermal oxide and subsequently coated by PECVD silicon nitride. Values for the emitter saturation current densities averaged on the whole wafer area of the samples are summarized in Table 1. Additionally, the limit of V_{oc} implied by j_{0e} is calculated (assuming j_{sc}=40 mA/cm²). It can be seen that the plasma ashing has no influence on the electrical quality. Both types of textures, random pyramids as well as the honeycomb texture, lead to increased values of j_{0e}, but they are on the same level. Therefore, it can be concluded that the electrical quality of the adapted process chain on large areas and using the Roller-NIL tool allows the fabrication of high efficiency solar cells.

Table I: Values for emitter saturation current density j_{0e} as well as thereby implied limits of $V_{oc.}$ For the honeycomb texture a mean value of 4 samples is given.

Sample type	j_{0e} [fA/cm²]	V_{oc} [mV]
Planar reference	121	687
Planar/Plasma ashing treatment	96	693
Random pyramids	151	681
Honeycomb texture	148	682

4 DIFFRACTIVE BACK SIDE GRATINGS

4.1 Master and stamp fabrication

Photoresist master structures again were originated using IL. This time, samples with linear and crossed symmetry were fabricated using the interference of two expanded laser beams. In case of the crossed grating samples a twofold exposure was conducted with a rotation of 90° of the sample in between. The basic principle of introducing back side grating structures in solar cells schematically is visualized in Fig.3. Diffraction effects lead to internal path length enhancements, which can be used to enhance especially the use of weakly absorbed light. Structure dimensions for both types of symmetry are around 1 µm period and are oriented to predicted optimal periods published in [13], [14]. The master sizes were 75x75 mm² and the pattern depth was around 350 nm.

Again PDMS stamps were replicated by cast moulding. However, for the smaller features given for this application, other PDMS recipes were applied. Here, a two layer stack of different PDMS components was applied. The thick bulk of the PDMS stamp is made of the same soft material as used in the application described before. On this bulk a comparably thin layer of about 30 µm of so-called h-PDMS is applied. This h-PDMS layer is used to replicate the master`s pattern. The development of h-PDMS is described in [18] and the fabrication of stacked PDMS layers was conducted according to [19].

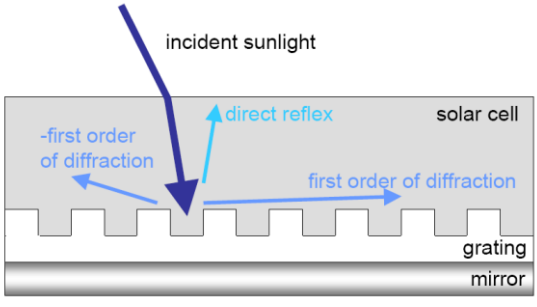

Figure 3: Sketch of the principle idea of back side gratings in silicon solar cells.

4.2 Nanoimprint lithography and plasma etching

In first tests, the NIL process for this application again was conducted using the conventional tool. An imprint process was set up using the mr-UVCur06 resist. Both for the linear as well as the crossed grating, very low residual layer thicknesses were achieved.

The plasma etching processes were investigated with the aim of realizing preferably binary grating profiles. This requires very anisotropic etching. For these smaller dimensions as for the application described before, very low pressures and thus high bias voltages in the RIE process were required. Corresponding process conditions were 1 Pa chamber pressure and a bias voltage around 300 V. Solely SF_6 was introduced into the chamber.

For the resist removal, two options were investigated. First, plasma ashing, and second, the dissolution of an adhesion promoter layer in an organic solvent was tested. Both options lead to satisfactory removal of the organic resist.

4.3 Optical and electrical characterisation

The optical characterization of textured solar cell precursors was already described in [20]. These precursors had a flat front surface with a silicon nitride ARC. On the rear side, the gratings were etched into the silicon and on the gratings silicon oxide layers were deposited differently. The task for applying a best possible dielectric buffer layer is to achieve a very level rear interface onto which the metallic rear reflector is deposited. Very high absorption enhancements above 50 % absolute at 1100 nm were measured. This was found for crossed gratings, which showed a better performance than linear gratings.

Since RIE processes, especially when applying high acceleration voltages, are known to deteriorate electrical material quality, we made use of a concept to decouple the electrical quality of the silicon bulk from the optically active grating. This is realized by passivating the planar rear side in a first step. Then, onto this passivated rear, an amorphous silicon layer is deposited, which subsequently is patterned by the presented process chain.

Lifetime samples were fabricated on FZ p-type 1 Ωcm material. The samples were passivated symmetrically by Al_2O_3 deposited via plasma enhanced atomic layer deposition (ALD). 300 nm a-Si layers were applied via PECVD onto the Al_2O_3 layer on both sides. The samples experienced an annealing process and then were characterized using quasi steady-state photoconductance (QSSPC). The results of these measurements were taken as reference to extract influences of the following patterning process. Therefore, single process steps of RIE and plasma ashing as well as combinations of NIL, RIE and plasma or wet chemical removal of the resist were performed on the samples and afterwards lifetimes were measured again. For each group three samples were characterized. The characterization of 7 groups (21 samples) leads to the conclusion that the texturisation process chain has no influence on the electrical quality. All samples showed a high lifetime level ranging from 1.1 ms to 2.1 ms initially as well as after the texturisation, with no significant trend visible for any process step or combination. Under the assumption of no change in the symmetry of the passivation quality, it can be concluded that surface recombination velocities for the passivated rear side in the range of 6 to 9 cm/s can be maintained even after introducing a photonic structure on the wafer rear (see Fig. 4). Thus, the concept of decoupling optical and electrical effects is verified.

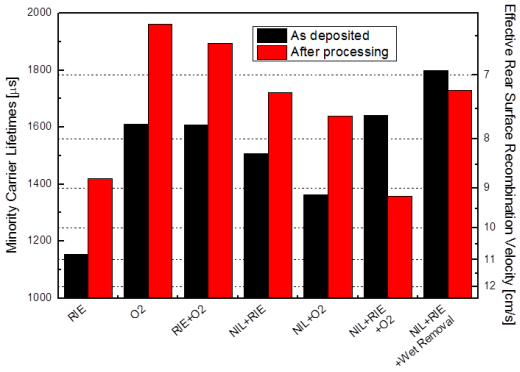

Figure 4: QSSPC measured lifetimes of symmetrically passivated samples before and after treatment with the listed process steps. Also shown are extracted values for S_{eff}. O_2 refers to plasma ashing of the photoresist.

Currently, work related to the contacting via laser-fired contacts (LFC) of the solar cell rear is ongoing [21]. The task here is to fire the aluminum through the dielectric buffer, the patterned a-Si and the Al_2O_3 layer. When these tests are completed, solar cells will processed, which are most likely to verify the beneficial absorption enhancement introduced by photonic structures in terms of an increased quantum efficiency in the long wavelength regime.

Besides these proof-of-concept studies, we are already in the up-scaling process for the imprinting of high resolution etching masks for this concept. To this end, stamps were fabricated with the purpose of realizing these etching masks using the Roller-NIL tool (see Fig. 5). Both pattern types, a linear and a crossed grating, were realized together on stamps. Thereby, the patterned area of one imprint is around 140x70 mm². This format does not yet allow the expression "full-wafer imprint"; however, it does show the potential of large area fabrication of high resolution etching masks. The fabrication of larger master structures via IL is not problematic and thus the final up-scaling of the patterning process for this concept will be tackled in future work.

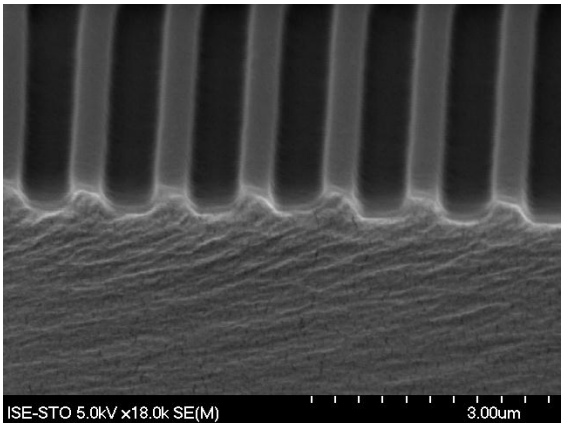

Figure 5: SEM micrograph of a linear grating with a period of 1 µm and a depth of about 300 nm imprinted using the Roller-NIL tool. In this case the initial resist thickness was not yet optimized leading to an overly residual layer beneath the imprinted pattern.

5 SUMMARY

High resolution defined textures can be realized using NIL processes. In the current paper, the up-scaling of NIL processes to continuous Roller-NIL processes is described. This technology opens up the possibility to introduce features as the honeycomb texture or even more visionary concepts as photonic structures into solar cell fabrication. The current status for both of these mentioned concepts based on the NIL processing at Fraunhofer ISE is described within this paper.

For the honeycomb texturing, the up-scaling to large area processing is already successfully demonstrated (156x156 mm² for NIL, 125x125 mm² for the plasma etching). Excellent optical properties close to pyramidal structures on c-Si were already reported and now also good electrical quality for the adapted process chain on large areas is verified.

The realization of photonic structures on the rear side of silicon solar cells based on NIL is also described. Excellent optical effects were already reported before and within this work, it is shown that the introduction of these diffractive features can be realized without affecting electrical properties. Beyond the device investigations based on the use of the conventional tool for NIL, first successful steps for the up-scaling to large areas using the Roller-NIL tool are described here.

Besides these applications, there is a wide range of fields of applications for this young technology to allow the realization of well-defined very fine features in solar cells. These could be of an optical nature to make use of resonant effects, up-conversion or plasmonics, but also non-optical applications could benefit by the options offered by NIL.

6 ACKNOWLEDGEMENT

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